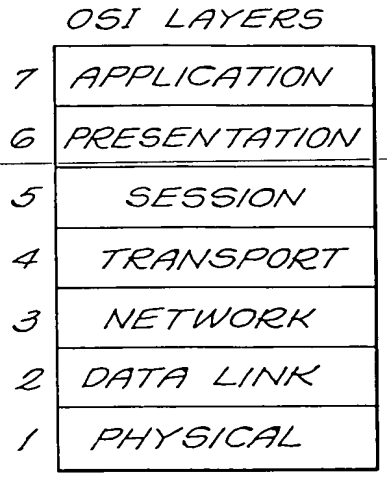

FIG. 1
(PRIOR ART)

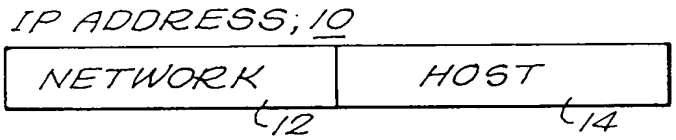

FIG. 2
(PRIOR ART)

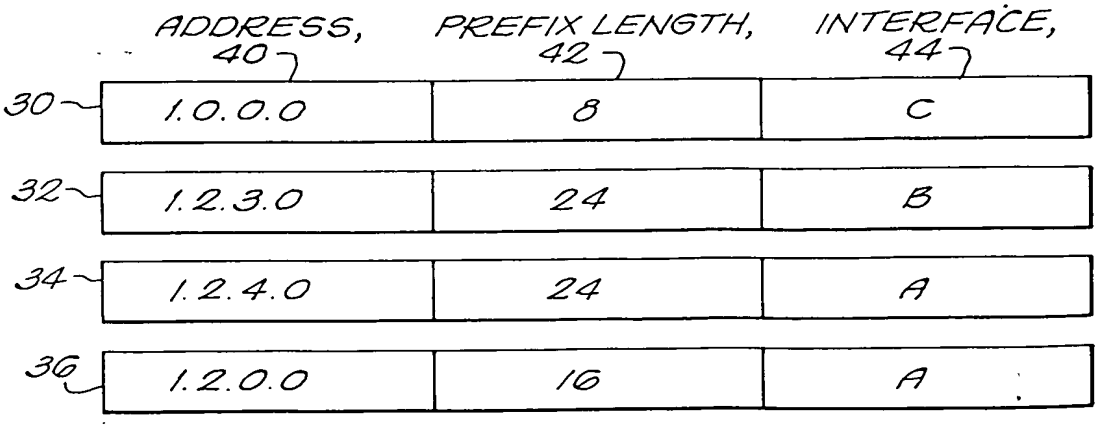

FIG. 4A
(PRIOR ART)

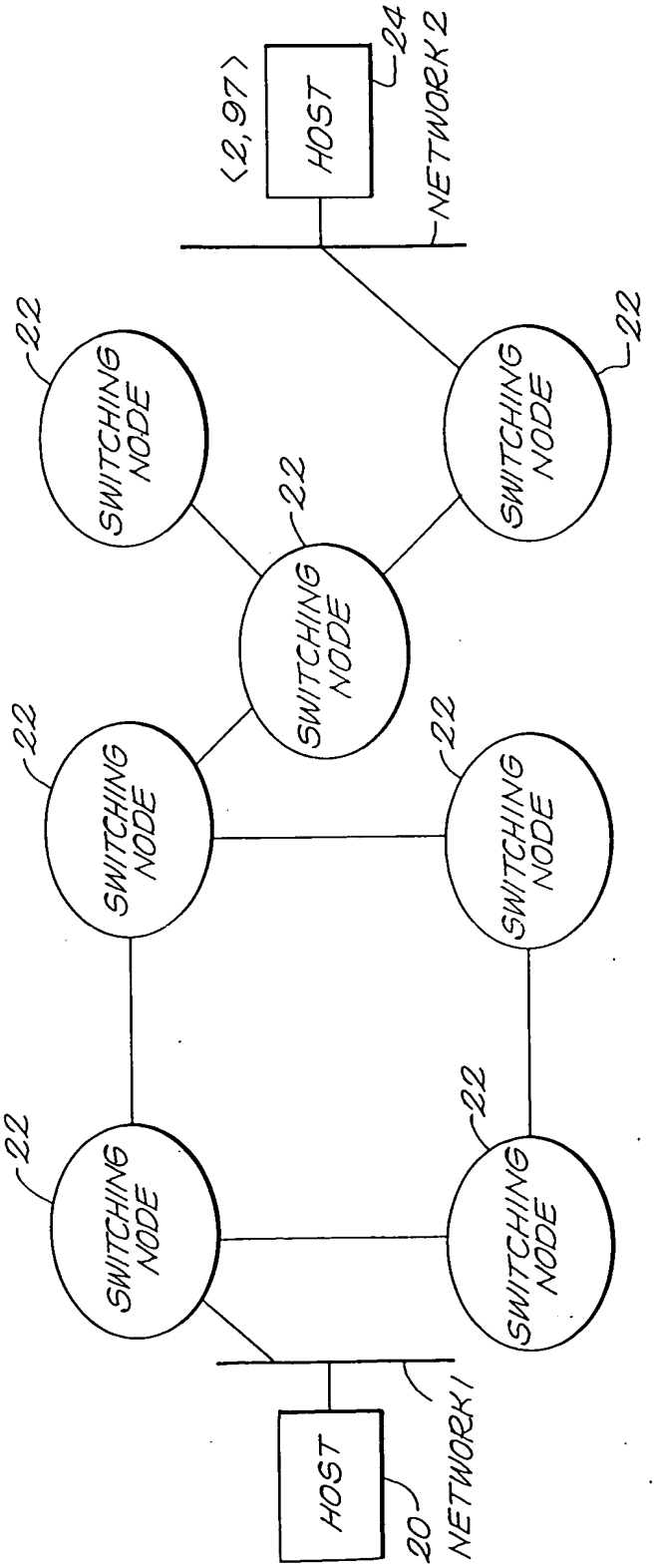

FIG. 3
(PRIOR ART)

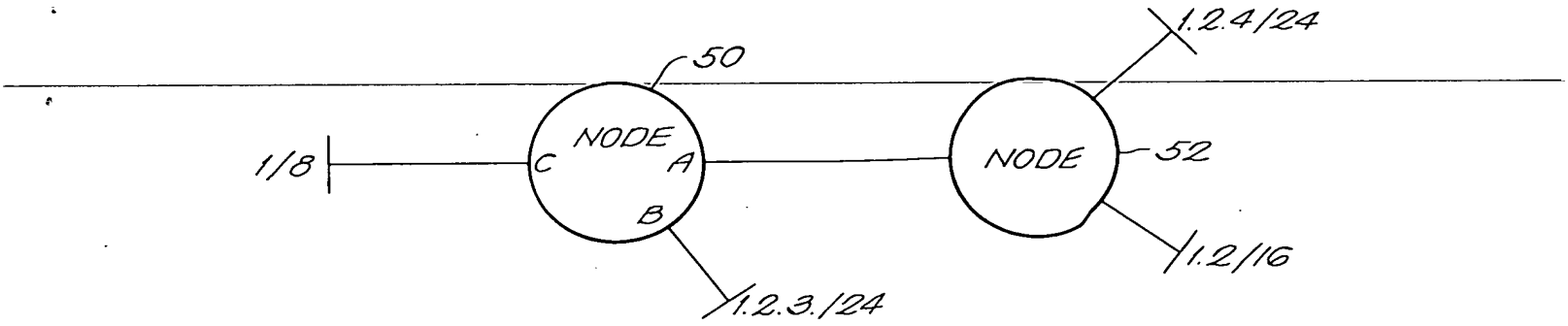

FIG. 4B
(PRIOR ART)

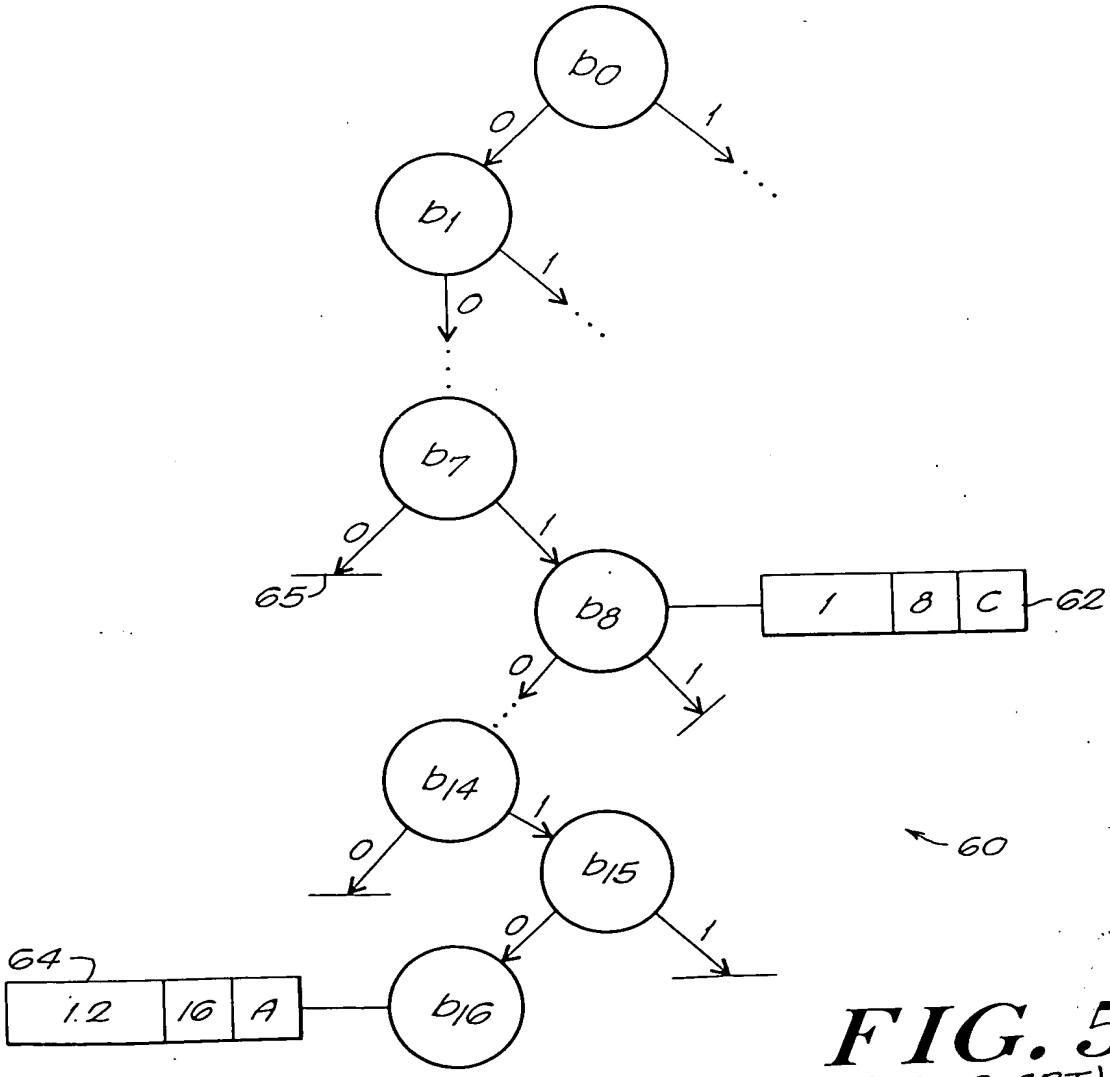

FIG. 5
(PRIOR ART)

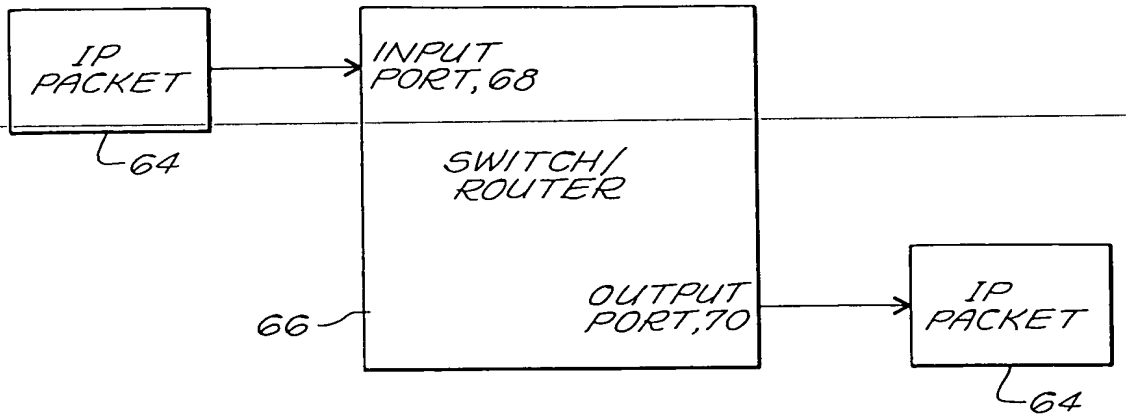
IP PACKET
64
INPUT PORT, 68
SWITCH/ ROUTER
66
OUTPUT PORT, 70
IP PACKET
64

FIG. 6

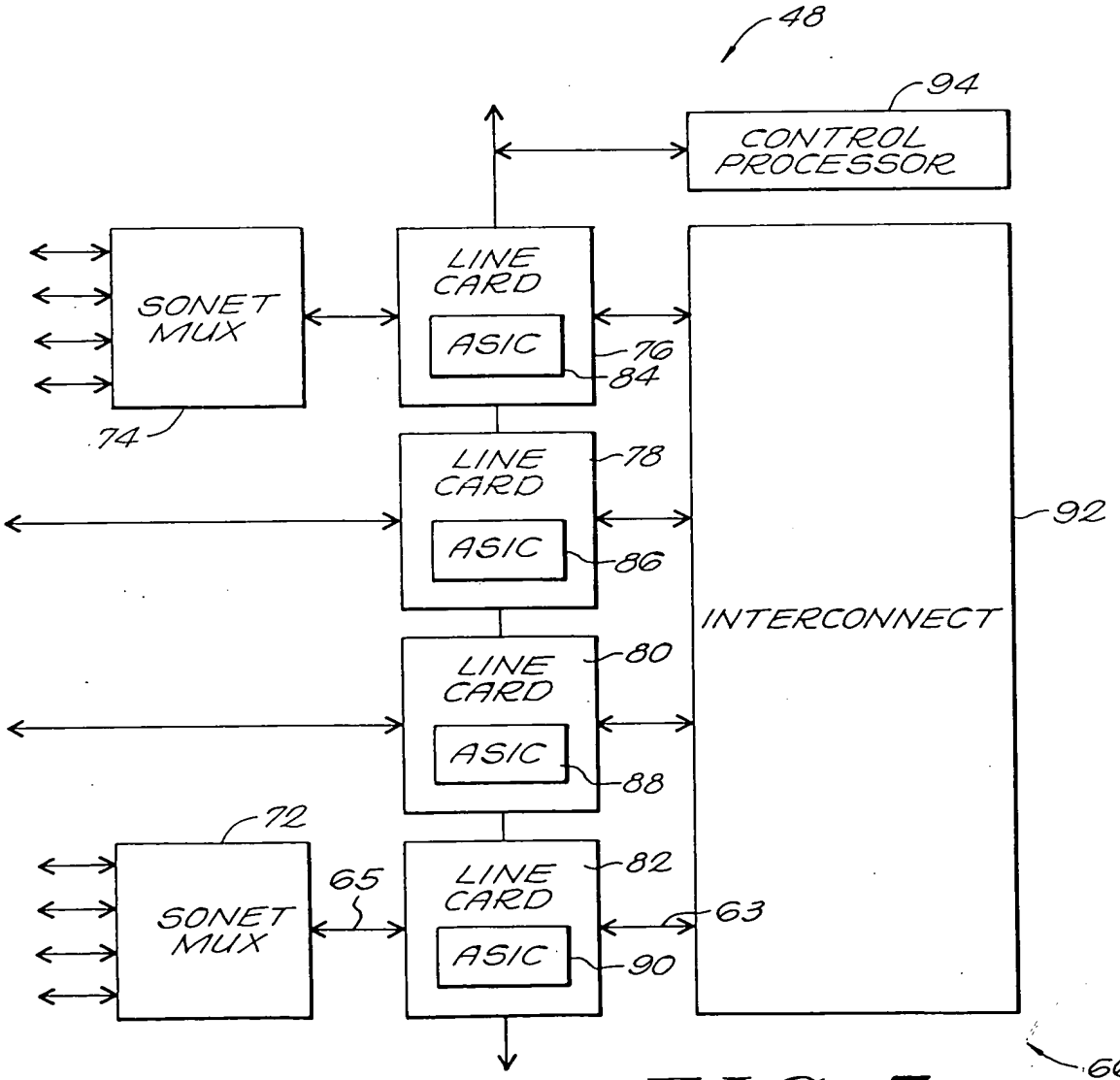
48
94
CONTROL PROCESSOR
SONET MUX
74
LINE CARD
ASIC
76
84
LINE CARD
78
ASIC
86
LINE CARD
80
ASIC
88
92
INTERCONNECT
72
SONET MUX
65
LINE CARD
82
ASIC
90
63
66

FIG. 7

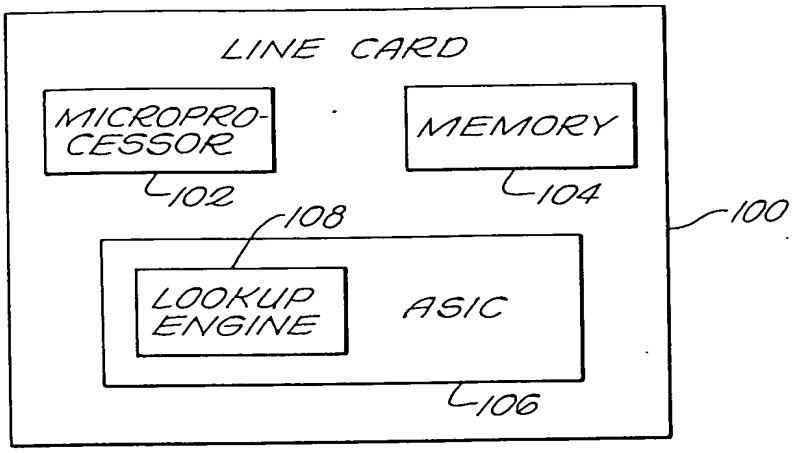
LINE CARD
MICROPRO-CESSOR
102
MEMORY
104
100
108
LOOKUP ENGINE
ASIC
106

FIG. 8

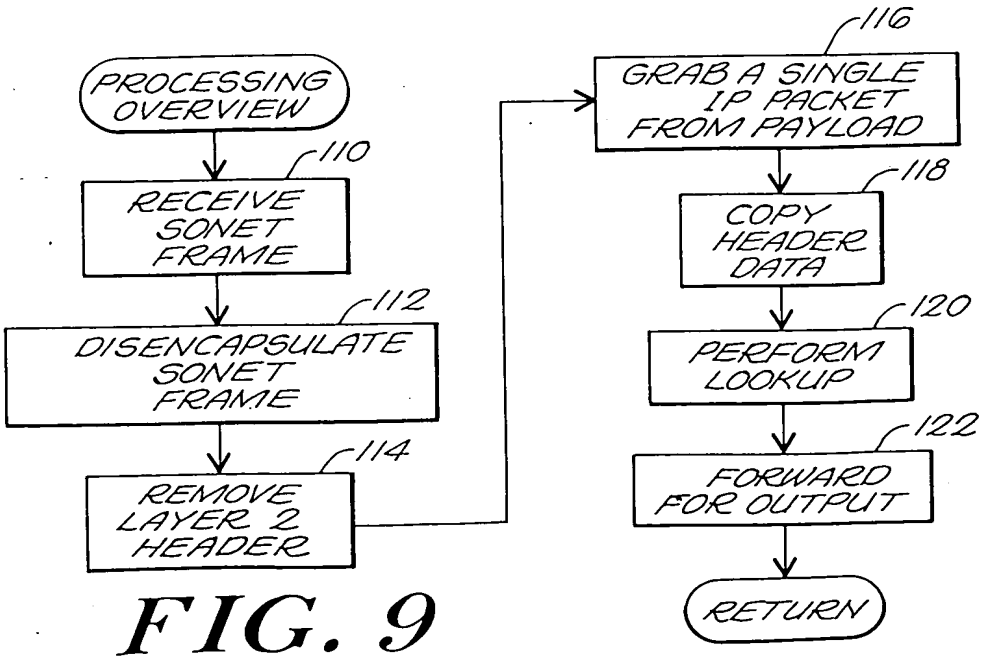
PROCESSING OVERVIEW
RECEIVE SONET FRAME
110
DISENCAPSULATE SONET FRAME
112
REMOVE LAYER 2 HEADER
114
GRAB A SINGLE IP PACKET FROM PAYLOAD
116
COPY HEADER DATA
118
PERFORM LOOKUP
120
FORWARD FOR OUTPUT
122
RETURN

FIG. 9

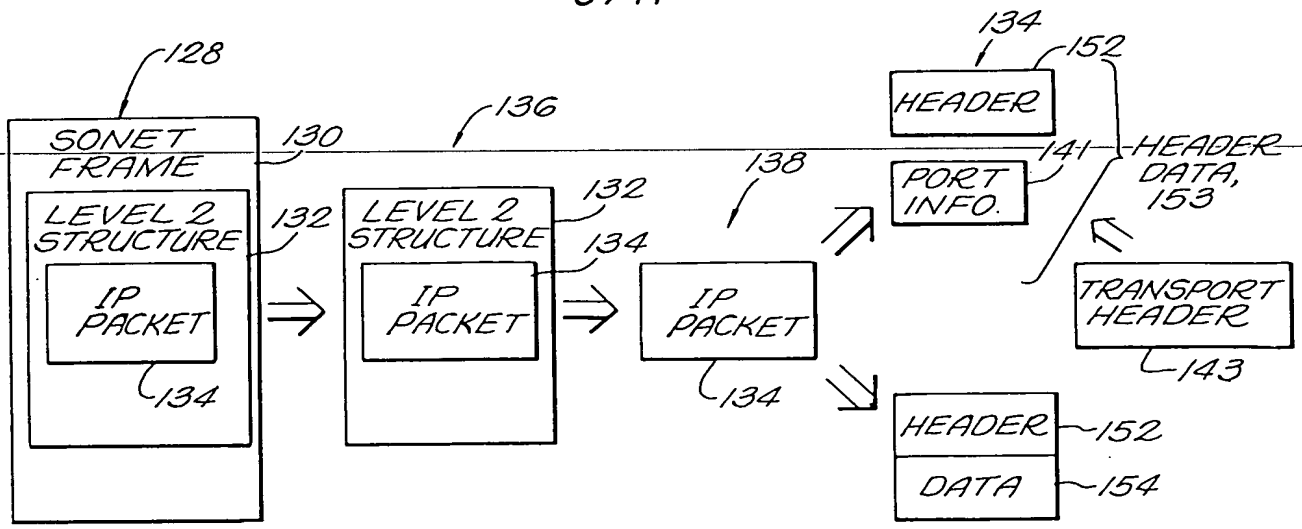

FIG. 10

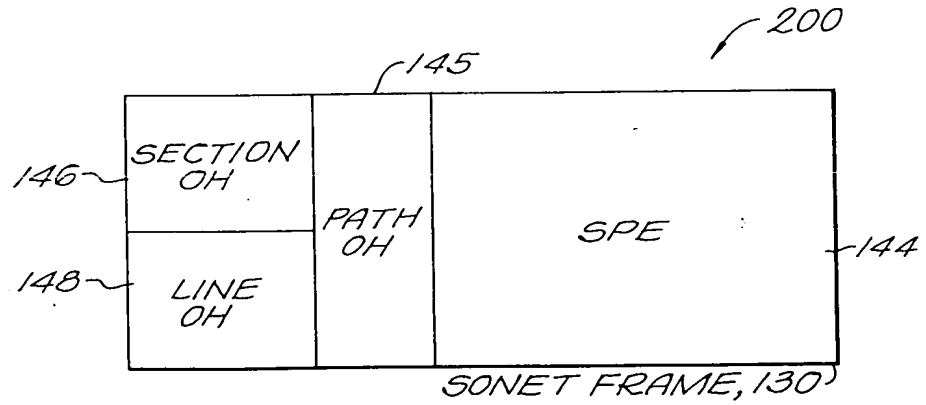

FIG. 11

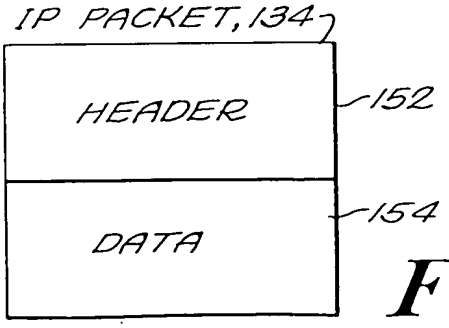

FIG. 12

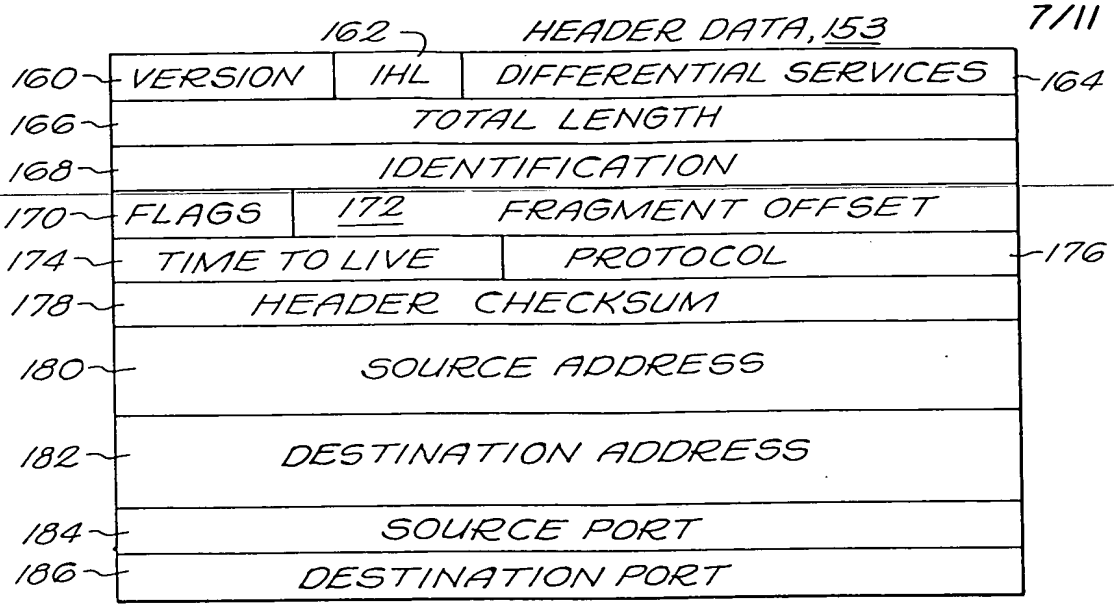

FIG. 13

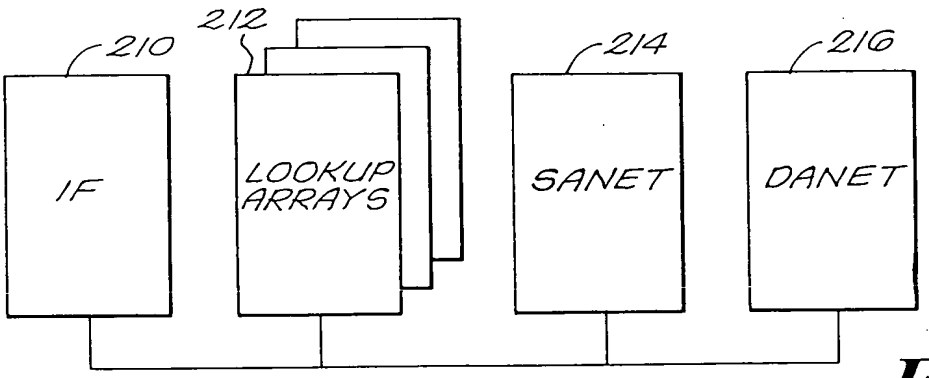

FIG. 14

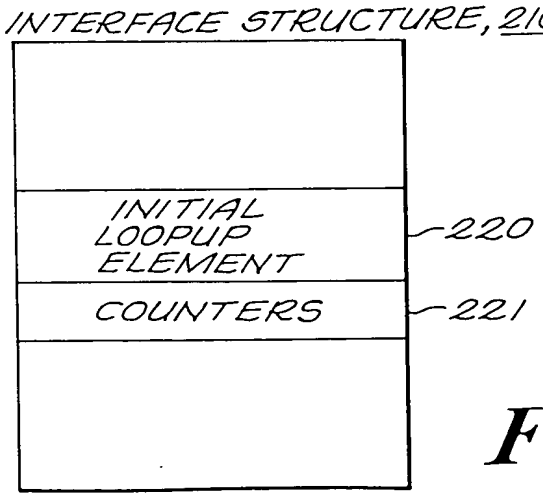

FIG. 15

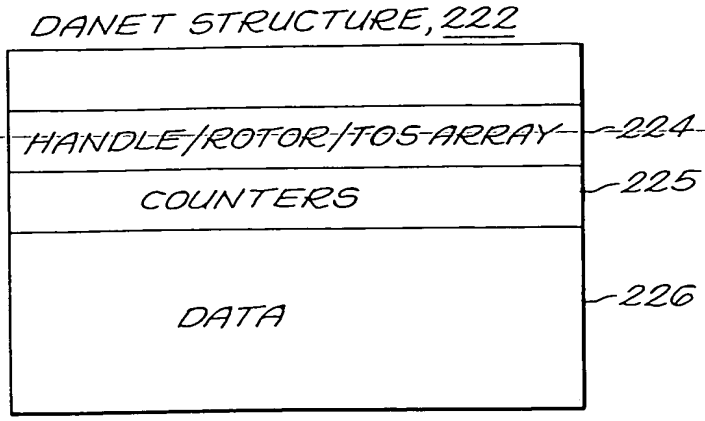
DANET STRUCTURE, 222
HANDLE/ROTOR/TOS-ARRAY
224
COUNTERS
225
DATA
226

FIG. 16

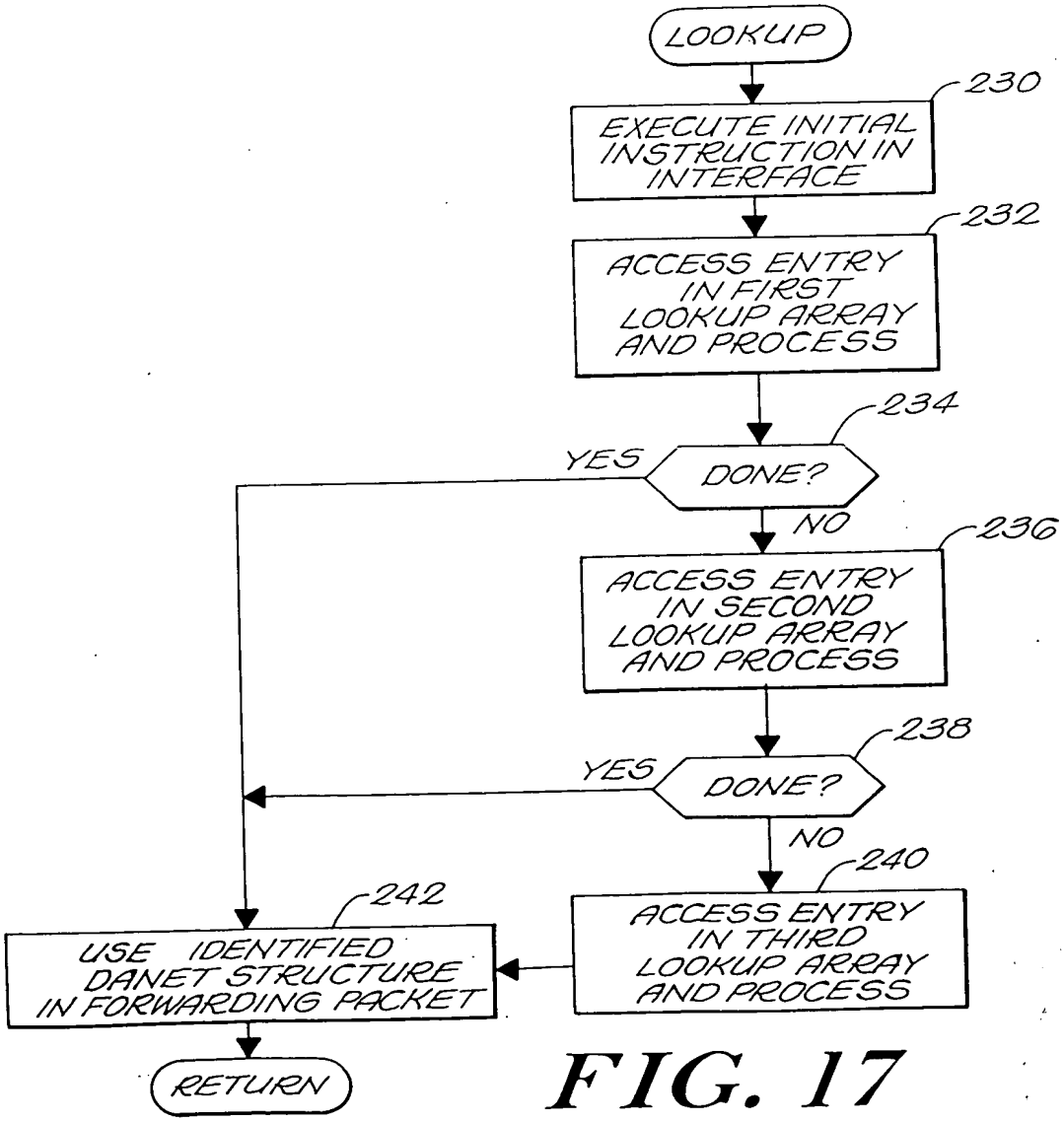
LOOKUP
EXECUTE INITIAL INSTRUCTION IN INTERFACE
230
ACCESS ENTRY IN FIRST LOOKUP ARRAY AND PROCESS
232
DONE?
234
YES
NO
ACCESS ENTRY IN SECOND LOOKUP ARRAY AND PROCESS
236
DONE?
238
YES
NO
ACCESS ENTRY IN THIRD LOOKUP ARRAY AND PROCESS
240
USE IDENTIFIED DANET STRUCTURE IN FORWARDING PACKET
242
RETURN

FIG. 17

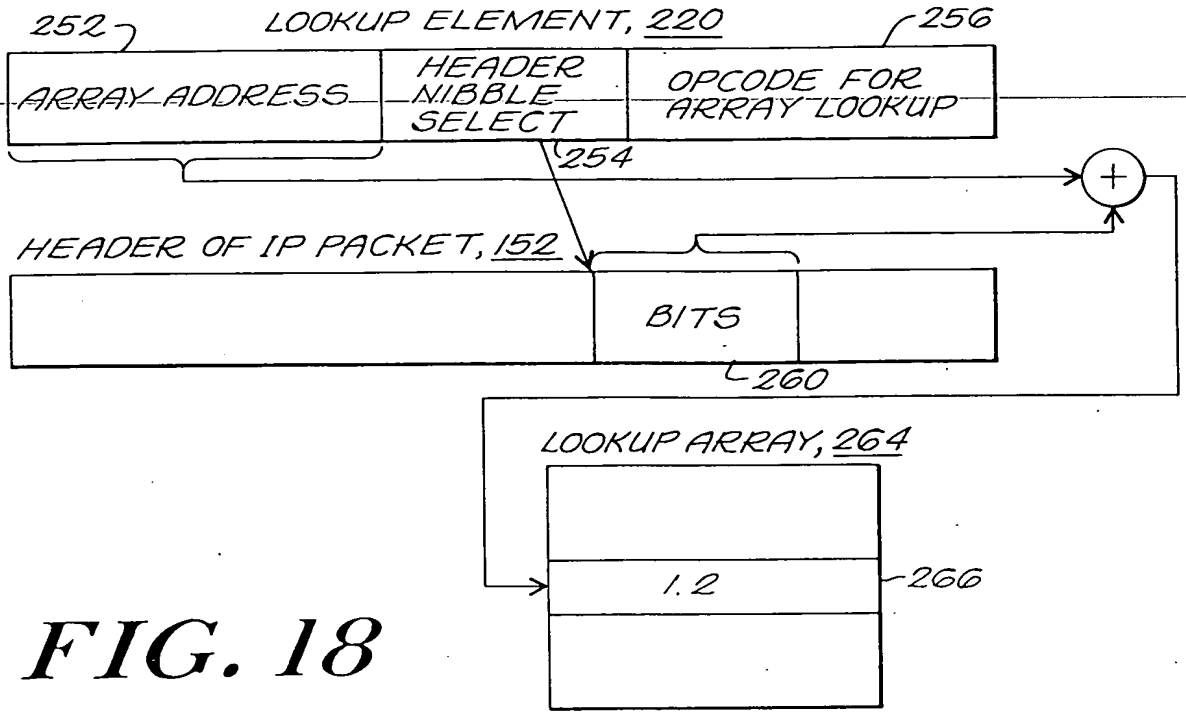

FIG. 18

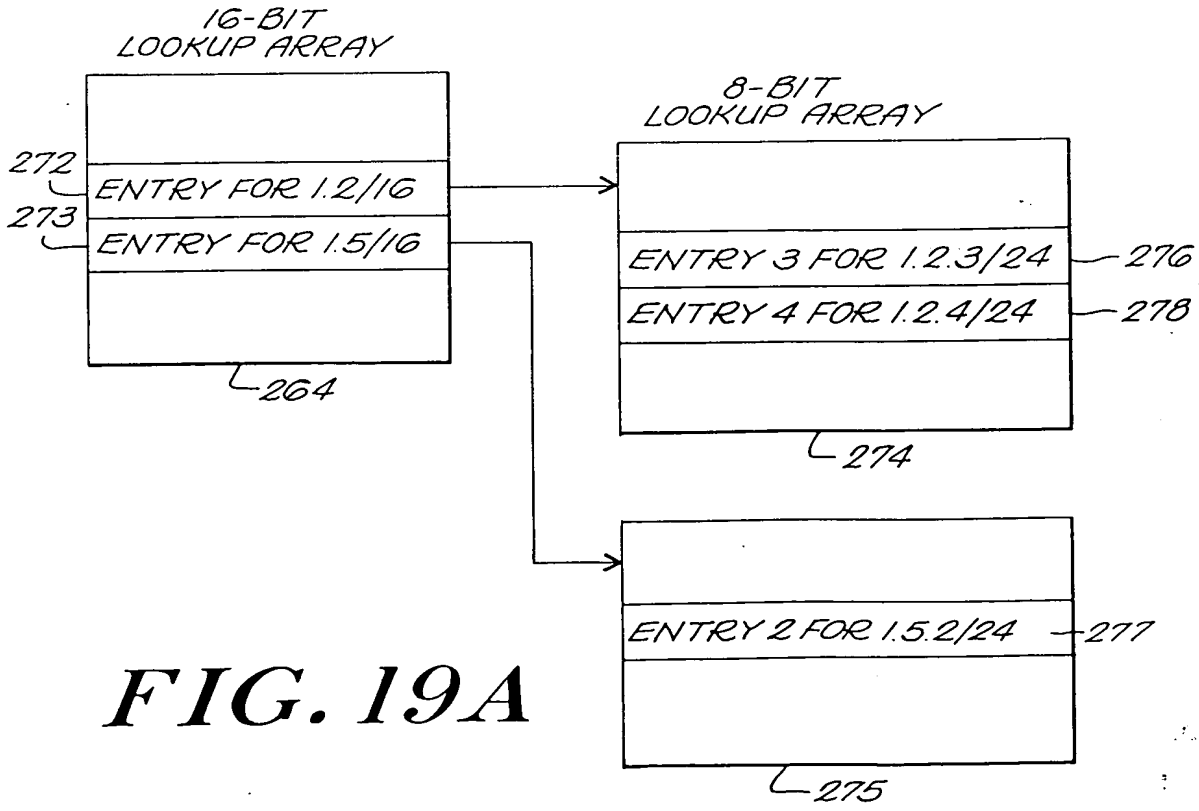

FIG. 19A

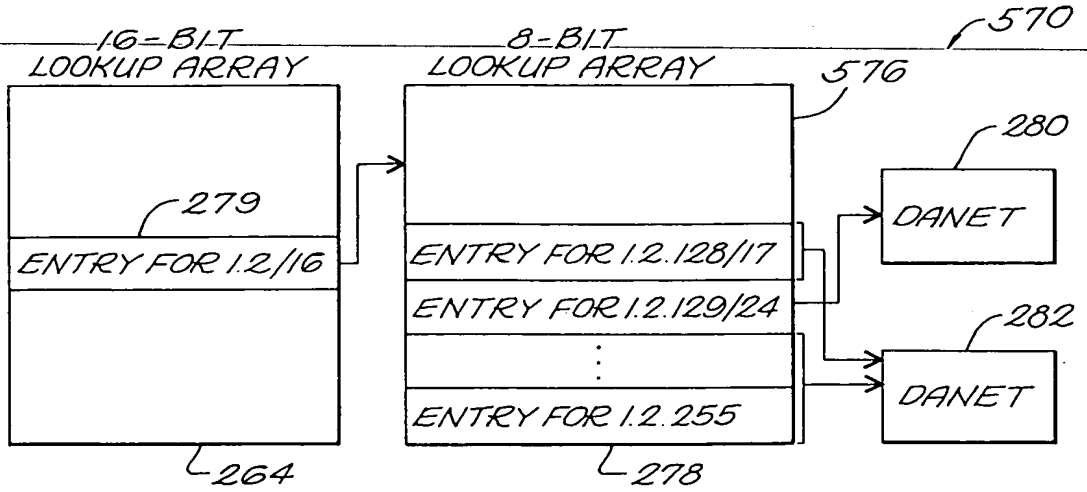

FIG. 19B

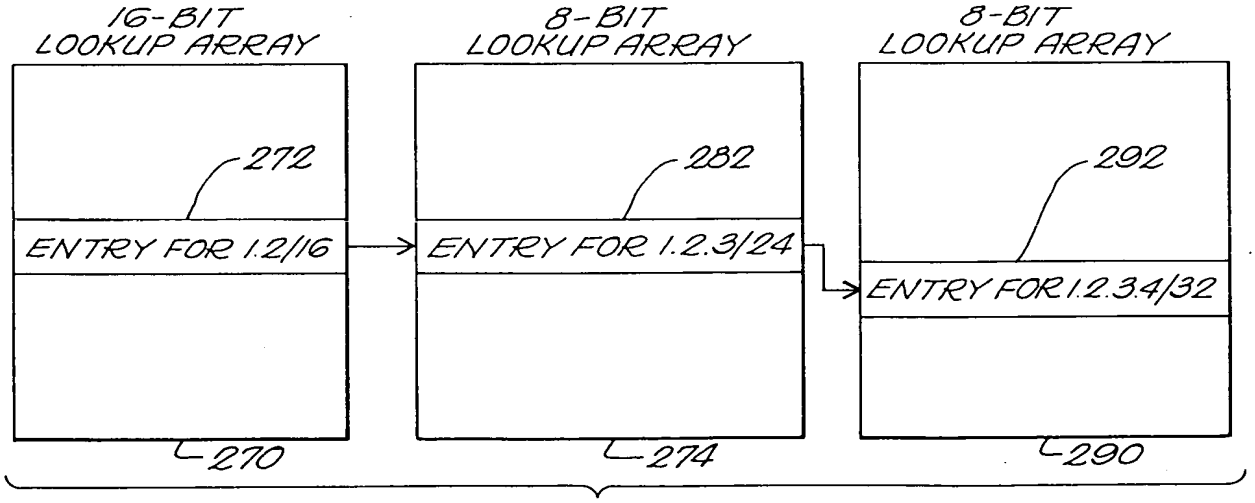

FIG. 19C

LOOKUP ELEMENT, 300

ARRAY ADDRESS	HEADER NIBBLE SELECT	OPCODE

FIG. 20

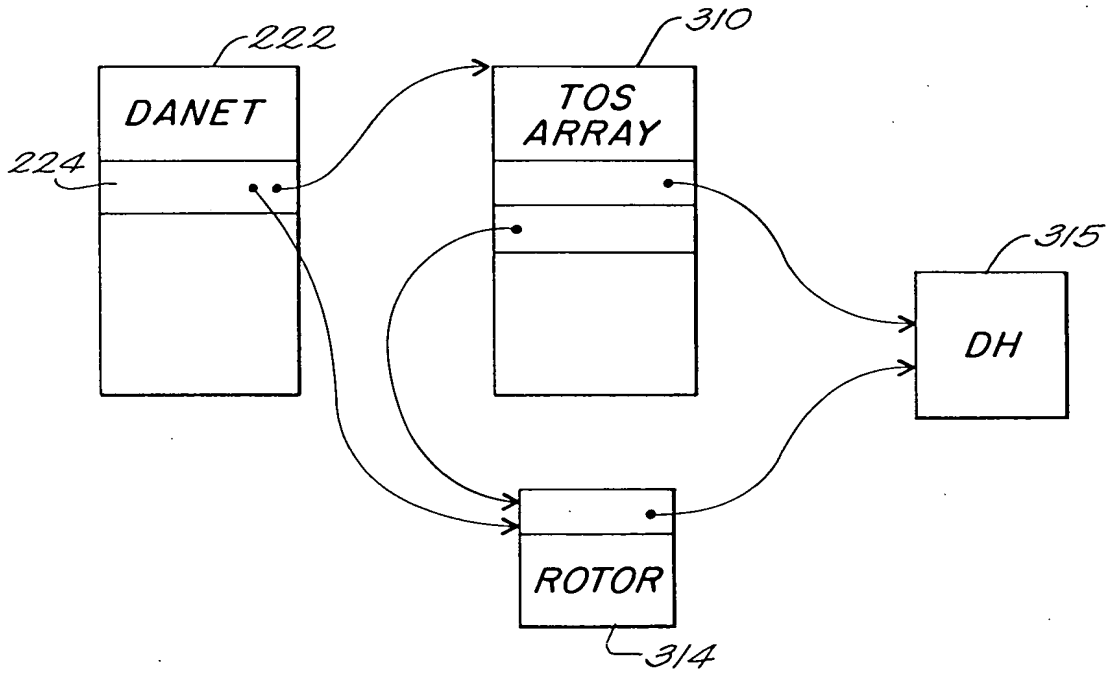

FIG. 21